| r No. | MTECH Network and internet engg |
|--|--|
| 1 | Find the missing term in the series: 3, 20, 63, 144, 275,? |
| Alt1 | |
| Alt2 | 468 |
| Alt3 | |
| Alt4 | |
| 7.10 | |
| 2 | Choose word from the given options which bears the same relationship to the third word, as the first two bears Anaemia: Blood :: Anarchy:? |
| Alt1 | Lawlesness |
| Alt2 | Government |
| | Monarchy |
| | Disorder |
| 7.1101 | 5.55.46. |
| 2 | Teeth is related to Grit in the same way as Fist is related to? |
| | Blow |
| | |
| | Hand |
| | Open St. 1 |
| Alt4 | Clench |
| | Select the lettered pair that has the same relationship as the original pair of words: Reproof: Scold Respite: Spite |
| Alt2 | Romantic: Strong |
| Alt3 | Salient: Prominent |
| Alt4 | Chastise: Erring |
| | |
| | Choose the alternative, which is similar to the given words: Bleat: Bray: Grunt |
| Alt1 | |
| | Croak |
| Alt3 | |
| | s^{\pm} I |
| | Scream |
| | Scream |
| Alt4 | |
| Alt4 | Spot the defective segment from the following: |
| Alt4 6 Alt1 | Spot the defective segment from the following: I wish |
| Alt4 6 Alt1 Alt2 | Spot the defective segment from the following: I wish I have a car |
| Alt4 6 Alt1 Alt2 Alt3 | Spot the defective segment from the following: I wish I have a car to go shopping |
| Alt4 6 Alt1 Alt2 Alt3 | Spot the defective segment from the following: I wish I have a car |
| Alt4 6 Alt1 Alt2 Alt3 Alt4 | Spot the defective segment from the following: I wish I have a car to go shopping in the rain Choose the meaning of the idiom/phrase from among the options given: |
| Alt4 6 Alt1 Alt2 Alt3 Alt4 | Spot the defective segment from the following: I wish I have a car to go shopping in the rain Choose the meaning of the idiom/phrase from among the options given: Out of sorts |
| Alt4 6 Alt1 Alt2 Alt3 Alt4 7 Alt1 | Spot the defective segment from the following: I wish I have a car to go shopping in the rain Choose the meaning of the idiom/phrase from among the options given: Out of sorts unwell |
| Alt4 6 Alt1 Alt2 Alt3 Alt4 7 Alt1 Alt2 | Spot the defective segment from the following: I wish I have a car to go shopping in the rain Choose the meaning of the idiom/phrase from among the options given: Out of sorts |

| | The way down at last days |
|---------|---|
| | The rowdy was at last done |
| | over |
| Alt2 | |
| | away |
| Alt4 | away with |
| | |
| 9 | Choose the option closest in meaning to the given word: |
| | BUCOLIC |
| - | rustic |
| | utopian |
| | peaceful |
| Alt4 | noisy |
| | |
| 10 | Choose the antonymous option you consider the best: |
| | CALLOW |
| Alt1 | immature |
| Alt2 | green |
| Alt3 | clumsy |
| Alt4 | veteran |
| | |
| 11 | If the seventh day of a month is three days earlier than Friday, what day will it be on the nineteenth day of the |
| | month? |
| Alt1 | Sunday |
| Alt2 | Monday |
| Alt3 | Wednesday |
| Alt4 | Friday |
| | |
| 12 | Water is related to Ocean in the same way as Snow is related to |
| Alt1 | Peaks |
| Alt2 | Hail |
| Alt3 | Glacier |
| Alt4 | Mountain |
| | |
| 13 | A's father's brother's father is D. how is D related to A? |
| Alt1 | Father |
| Alt2 | Grandfather |
| Alt3 | Uncle |
| Alt4 | Son |
| | |
| 14 | Find the odd man out: |
| | Squash |
| | football |
| | hockey |
| | Cricket |
| , | 1-11-11-11 |

| 15 | In a certain code language, if CRICKET is coded as 3923564, ROCKET is coded as 913564 and KETTLE is coded as |
|-------|--|
| | 564406, then how is LITTLE coded in that language ? |
| Alt1 | 024406 |
| Alt2 | 240406 |
| | 20446 |
| Alt4 | 200446 |
| | |
| 16 | |
| | 80 degrees |
| | 90 degrees |
| | 100 degrees |
| Alt4 | 120 degrees |
| 17 | Odd one out 2.4 6.9 |
| Alt1 | Odd one out: 2,4,6,8 |
| Alt1 | |
| Alt3 | |
| Alt4 | |
| 71104 | <u> </u> |
| 18 | Which is smallest: |
| | Quarter of 140 |
| | Double of 4*4 |
| Alt3 | 7*5 |
| Alt4 | Half of 72 |
| | |
| 19 | What is the next alphabet in the following series |
| | Z D X H V L T ? |
| Alt1 | Q |
| Alt2 | |
| Alt3 | |
| Alt4 | 0 |
| | |
| | How many times is the abbrevations FB shorter than the word FACEBOOK? |
| | 4times |
| | 3times 5times |
| | Many |
| AIL4 | IMATTY |
| 21 | The value of the postfix expression 5 6 3 * + 2 4 * + is |
| Alt1 | |
| Alt2 | |
| | 120 |
| Alt4 | |
| | |
| 22 | Which of the following sorting method is suitable for applications where the input is too large to fit into |
| | memory? |
| Alt1 | Shell sort |
| | |

| A I+2 | Quick sort |
|---------|--|
| | |
| | Bubble sort |
| Alt4 | Polyphase merge |
| | |
| 23 | The type of algorithm in which a decision is made that appears to be good, without regard for future |
| | consequences is called |
| | Greedy algorithm |
| | Pre emptive algorithm |
| | Non-Pre emptive algorithm |
| Alt4 | Branch and bound algorithm |
| 1 | |
| 24 | Rapid Application Development is an software process model. |
| Alt1 | Incremental |
| Alt2 | Universal Prescriptive |
| Alt3 | Initial classical |
| Alt4 | Evolutionary |
| | |
| 25 | is qualitative measures of degree to which classes are connected to each other. |
| Alt1 | Abstraction |
| Alt2 | Cohesion |
| Alt3 | Coupling |
| | Elicitation |
| | |
| 26 | Equivalence partitioning is a testing method. |
| | White Box |
| | Green Box |
| | Black Box |
| | Basic path |
| 7.110.1 | |
| 27 | Which of the following statement is true? |
| | If a language is context free it can always be accepted by a deterministic push-down automaton |
| | The complement of a context free language is context free |
| | The union of two context free languages is context free |
| | The intersection of two context free languages is context free |
| All4 | The intersection of two context free languages is context free |
| 20 | Correct hierarchical relationship among context- free, right-linear, and context-sensitive language is |
| 20 | Correct meral chical relationship among context- free, right-linear, and context-sensitive language is |
| Λ l+1 | context-free ⊂ right-linear ⊂ context-sensitive |
| | context-free ⊂ context-sensitive ⊂ right-linear |
| | |
| | context-sensitive ⊂ right-linear ⊂ context-free |
| Alt4 | right-linear ⊂ context-free ⊂ context-sensitive |
| 20 | Lat 7 (a b a d a) The number of strings in 7% of length 4 such that are sumballicured asset that are |
| | Let $\Sigma = \{a, b, c, d, e\}$. The number of strings in Σ^* of length 4 such that no symbol is used more than once in a |
| | string is |
| Alt1 | |
| Alt2 | |
| Alt3 | 35 |

| Alt4 | |
|-------|--|
| 22 | The fallenting CEC is in |
| | The following CFG is in |
| | S → aBB |
| | $B \rightarrow bAA$ |
| | $A \rightarrow a$ |
| | B 	o b |
| | |
| Alt1 | Chomsky normal form but not strong Chomsky normal form |
| Alt2 | Weak Chomsky normal form but not Chomsky normal form |
| Alt3 | Strong Chomsky normal form |
| | Greibach normal form |
| | |
| 31 | Which of the following is the most powerful parser? |
| Alt1 | |
| | LALR |
| | Canonical LR |
| | |
| Alt4 | operator-precedence |
| | |
| | In a compiler, keywords of a language are recognized during |
| | Data flow analysis |
| Alt2 | parsing of the program written |
| Alt3 | the lexical analysis of the program |
| Alt4 | the code generation |
| | |
| 33 | Consider the grammar: E ::= E+E E*E (E) a |
| | The number of right most derivation for the sentence (a) is |
| | |
| Alt1 | 2 |
| Alt2 | 4 |
| Alt3 | |
| Alt4 | |
| 7.10. | <u>-</u> |
| 34 | Which of the following intermediate best suited for derivation of common sub-expression? |
| | triples |
| | trees |
| | |
| | qudraples postfix code |
| AIL4 | postrix code |
| 2.5 | DVCT stands for |
| | DVST stands for |
| | Digital View Storing Table |
| | Direct Visual Storage Tube |
| | Direct View Storage Tube |
| Alt4 | Digital View Storage Tube |
| - | |
| 36 | Resources are allocated to the process on non-sharable basis is called |
| Alt1 | Non Pre-Emption |

| Alt2 | Mutual exclusion |
|----------|--|
| Alt3 | Hold and wait |
| Alt4 | Pre-Emption |
| | |
| 37 | In Round Robin CPU scheduling, as time quantum is increased the average turn-around time |
| Alt1 | Remains constant |
| Alt2 | Decreases |
| Alt3 | Varies irregularly |
| Alt4 | Increases |
| | |
| 38 | A system has n resources of same type. These resources are shared by 3 processes P1, P2, and P3 which have peak demands 3, 4, and 5 respectively. For what value of n deadlock will not occur? |
| Alt1 | 7 Resources |
| - | 9 Resources |
| Alt3 | 10 Resources |
| - | 13 Resources |
| | |
| 39 | Banker's algorithm for resource allocation deals with |
| | Mutual exclusion |
| Alt2 | Deadlock recovery |
| | Deadlock prevention |
| - | Compiler Optimization |
| <u> </u> | |
| 40 | Distributed OS works on the principle. |
| | File Foundation |
| Alt2 | Multi system image |
| | Single System image |
| | Networking image |
| | |
| 41 | Signals that run from 0 up to a maximum frequency are called . |
| | Pause band signals |
| | Radio Signals |
| | Maximum frequency Signals |
| | Base band signals |
| | |
| 42 | A computer on a 6-Mbps network is regulated by a token bucket. The token bucket is filled at the rate of 1 Mbps. It is initially filled to capacity with 10 megabits. How long can the computer transmit at the full 6 Mbps? |
| Alt1 | 2 seconds |
| Alt2 | 5 seconds |
| | 8 seconds |
| - | 10 seconds |
| | |
| 43 | The language accepted by a Push Down Automata is |
| | Type 0 |
| - | Type 1 |
| L | L-11 |

| Alt3 | Type 4 |
|------|--|
| Alt4 | Type 2 |
| | |
| 44 | Non-modifiable procedures are called |
| Alt1 | Concurrent procedures |
| Alt2 | Serially usable procedures |
| Alt3 | Re-entrant procedures |
| Alt4 | Top-down procedures |
| | |
| 45 | DBMS provides the facility of accessing data from a database through |
| Alt1 | DDL |
| Alt2 | DML |
| Alt3 | DBA |
| Alt4 | Schema |
| | |
| 46 | A weak entity type always has |
| Alt1 | Partial participation constraint |
| Alt2 | No participation constraint |
| Alt3 | Total participation constraint |
| Alt4 | Either partial or total participation constraint |
| | |
| 47 | Which of these is a characteristic of RAID 5? |
| Alt1 | Dedicated parity |
| Alt2 | Double parity |
| Alt3 | Hamming code parity |
| Alt4 | Distributed parity |
| | |
| 48 | signal prevents the microprocessor from reading the same data more than one. |
| Alt1 | Pipelining |
| Alt2 | Handshaking |
| Alt3 | Controlling |
| Alt4 | Alert |
| | |
| 49 | The RST7 instruction in 8085 microprocessor is equal to |
| Alt1 | CALL 0010 H |
| Alt2 | CALL 0034 H |
| Alt3 | CALL 0038 H |
| Alt4 | CAL 003C H |

```
50
     What is the output of the program in C?
     #include<stdio.h>
     main()
     {
     int a=10;
     int b=20;
     a= a+b;
     b = a - b;
     a= a-b;
     printf("%d%d", a, b);
     }
Alt1 20, 10
Alt2 10, 10
Alt3 10, 20
Alt4 20, 30
```

| 51 | The number of edges in a regular graph of degree'd' and 'n' vertices is |
|------|---|
| Alt1 | Maximum of n,d |
| Alt2 | n+d |
| Alt3 | nd |
| Alt4 | nd/2 |

| 52 | The number of possible binary tree with 4 nodes is |
|------|--|
| Alt1 | 12 |
| Alt2 | 14 |
| Alt3 | 16 |
| Alt4 | 24 |

```
The following program fragment
53
            int a = 4, b = 6;
             printf("%d", a!=b);
```

| | The following program fragment |
|------|--|
| | int a = 4, b = 6; printf("%d", a!=b); |
| Alt1 | Outputs an error message |
| Alt2 | Prints 0 |
| Alt3 | Prints 1 |
| Alt4 | Garbage value |

| 54 | The FSM pictured in the below figure recognize the |
|------|---|
| | |
| | |
| | |
| | |
| | |
| | |
| Alt1 | Any string of odd number of a's |
| Alt2 | Any string of odd number of a's and even number of b's |
| Alt3 | Any string of even number of a's and even number of b's |
| Alt4 | Any string of odd number of a's and odd number of b's |

| 55 | Shift-Reduce parsers are |
|------|-------------------------------------|
| Alt1 | Top-down parser |
| Alt2 | Bottom-up parser |
| Alt3 | May be top-down or bottom-up parser |
| Alt4 | None of the above |

| | Consider six memory partitions of sizes 200KB, 400KB, 600KB, 500KB, 300KB and 250KB, where KB refers to Kilobyte. These partition needs to be allotted to four processes of sizes 357KB, 210KB, 468KB and 491KB in that order. If best fit algorithm is used, which partitions are not allotted to any process? |
|------|---|
| Alt1 | 200KB and 300KB |
| Alt2 | 200KB and 250KB |
| Alt3 | 250KB and 300KB |
| Alt4 | 300KB and 400KB |

| 57 | An optimizing compiler |
|----|------------------------|
| | |

| Alt1 | Is optimized to take less time for execution |
|------------|---|
| Alt2 | Is optimized to occupy less space |
| Alt3 | Optimized the code |
| Alt4 | None of the above |
| | |
| 58 | A resource-management platform responsible for managing computing resources in clusters and using them |
| | for scheduling of users' applications in hadoop environment |
| Alt1 | Hadoop HDFS |
| Alt2 | Hadoop MapReduce |
| Alt3 | Hadoop Common |
| Alt4 | Hadoop Yarn |
| | |
| 59 | In distributed systems, link and site failure is detected by |
| Alt1 | Polling |
| Alt2 | Handshaking |
| Alt3 | token passing |
| Alt4 | Token sharing |
| | |
| 60 | The potential overuse of a single parity disk is avoided in RAID level |
| Alt1 | 5 |
| Alt2 | 4 |
| Alt3 | 3 |
| Alt4 | 2 |
| | |
| 61 | A system is in a safe state only if there exists a: |
| Alt1 | safe allocation |
| Alt2 | safe resource |
| Alt3 | safe sequence |
| Alt4 | All of these |
| | |
| 62 | A transformation that slants the shape of an object is called |
| Alt1 | Reflection |
| Alt2 | Shear |
| Alt3 | Distortion |
| Alt4 | Scaling |
| | |
| 63 | What is the natural mask for class-c network |
| Alt1 | 255.255.255.1 |
| Alt2 | 255.255.255.0 |
| Alt3 | 255.255.255 |
| Alt4 | 255.255.254 |
| | |
| | A system has 6 identical resources and N processes competing for them. Each process can request at most 2 |
| 64 | respectively and the first and the processes competing for them. Each process can request at most 2 |
| 64 | resources. Which one of the following values of N could lead to a deadlock? |
| 64 Alt1 | resources. Which one of the following values of N could lead to a deadlock? |
| | resources. Which one of the following values of N could lead to a deadlock? 1 |

Alt4 4

```
Consider the following function written in C programming language

void foo(char *a) {

if( *a && *a != ' ') {

foo(a+1);

putchar(*a)

}

The output of the above function on input "ABCD EFGH" is

Alt1 ABCD EFGH

Alt2 ABCD

Alt3 HGFE DCBA

Alt4 DCBA
```

| Considert | he following relation | ons A, B and C: |
|--------------|-----------------------|-----------------|
| Α | В | C |
| ID Name Ag | e ID Name Age | Id Phone Area |
| 12 Arun 60 | 15 Shreya 24 | 10 2200 02 |
| 15 Shreya 24 | 25 Hari 40 | 99 2100 01 |
| 99 Rohit 11 | 98 Rohit 20 | |
| | 99 Rohit 11 | |

Alt3 5

| | | | ne following SQL query contain? LL (SELECT B.Age FROM B WHERE B.Name = 'Arun') |
|------|---|------------------|--|
| | Consider the fo | llowing relation | ons A, B and C: |
| | А | В | С |
| | ID Name Age ID | Name Age | Id Phone Area |
| | 12 Arun 60 15 | Shreya 24 | 10 2200 02 |
| | 15 Shreya 24 25 | Hari 40 | 99 2100 01 |
| | 99 Rohit 11 98 | Rohit 20 | |
| | 99 1 | Rohit 11 | |
| | | | |
| Alt1 | 4 | | |
| Alt2 | | | |
| Alt3 | | | |
| Alt4 | 1 | | |
| 68 | A RAM chip has a capaci needed to construct a 16 | • | rds of 8 bits each (1K \times 8). The number of 2 \times 4 decoders with enable om 1K \times 8 RAM is |
| Alt1 | | | |
| Alt2 | 5 | | |
| Alt3 | 6 | | |
| Alt4 | 7 | | |
| | | | |
| 69 | | _ | ne cable (in km) for transmitting data at a rate of 500 Mbps in an Eth sume the signal speed in the cable to be 2,00,000 km/s. |
| Alt1 | 1 | | |
| Alt2 | | | |
| Alt3 | 2.5 | | |
| Alt4 | 5 | | |
| | | | |

after each stage and the delay of each buffer is 1 ns. A program consisting of 12 instructions I1, I2, I3, ..., I12 is executed in this pipelined processor. Instruction I4 is the only branch instruction and its branch target is I9. If the

branch is taken during the execution of this program, the time (in ns) needed to complete the program is

| Alt1 | 132 | |
|--|--|---|
| Alt2 | 165 | |
| Alt3 | 176 | |
| Alt4 | 328 | |
| 71 | | |
| | Match t | the following: |
| | 1) Waterfall model | a) Specifications can be developed incrementally |
| | 2) Evolutionary model | b) Requirements compromises are inevitable |
| | 3) Component-based software engineering | c) Explicit recognition of risk |
| | 4) Spiral development | d) Inflexible partitioning of the project into stages |
| Alt1 | 1-a, 2-b, 3-c, 4-d | |
| Alt2 | 1-d, 2-a, 3-b, 4-c | |
| | 1 4, 2 4, 3 5, 4 6 | |
| Alt3 | 1-d, 2-b, 3-a, 4-c | |
| Alt3 | | |
| Alt3 | 1-d, 2-b, 3-a, 4-c 1-c, 2-a, 3-b, 4-d In designing a computer's cache system, the cache | · · · · · · · · · · · · · · · · · · · |
| Alt4 | 1-d, 2-b, 3-a, 4-c 1-c, 2-a, 3-b, 4-d | · · · · · · · · · · · · · · · · · · · |
| Alt3 Alt4 72 Alt1 | 1-d, 2-b, 3-a, 4-c 1-c, 2-a, 3-b, 4-d In designing a computer's cache system, the cache one of the following statements is correct in this cor A smaller block size implies better spatial locality | ntext? |
| Alt3 Alt4 72 Alt1 Alt2 | 1-d, 2-b, 3-a, 4-c 1-c, 2-a, 3-b, 4-d In designing a computer's cache system, the cache one of the following statements is correct in this cor | e lower cache tag overhead |
| Alt3 Alt4 72 Alt1 Alt2 Alt3 | 1-d, 2-b, 3-a, 4-c 1-c, 2-a, 3-b, 4-d In designing a computer's cache system, the cache one of the following statements is correct in this cor A smaller block size implies better spatial locality A smaller block size implies a smaller cache tag and hence | e lower cache tag overhead |
| Alt3 Alt4 72 Alt1 Alt2 Alt3 Alt4 73 | 1-d, 2-b, 3-a, 4-c 1-c, 2-a, 3-b, 4-d In designing a computer's cache system, the cache one of the following statements is correct in this cornect in this c | e lower cache tag overhead lower cache hit time TU) of 1500 bytes has received an IP packet of size 4404 es of the relevant fields in the header of the third IP |
| Alt3 Alt4 72 Alt1 Alt2 Alt3 Alt4 73 | 1-d, 2-b, 3-a, 4-c 1-c, 2-a, 3-b, 4-d In designing a computer's cache system, the cache one of the following statements is correct in this cor A smaller block size implies better spatial locality A smaller block size implies a smaller cache tag and hence A smaller block size implies a larger cache tag and hence A smaller block size incurs a lower cache miss penalty An IP router with a Maximum Transmission Unit (M bytes with an IP header of length 20 bytes. The value fragment generated by the router for this packet are MF bit: 0, Datagram Length: 1444; Offset: 370 | e lower cache tag overhead lower cache hit time TU) of 1500 bytes has received an IP packet of size 4404 es of the relevant fields in the header of the third IP |
| Alt3 Alt4 72 Alt1 Alt2 Alt3 Alt4 73 Alt1 Alt2 | 1-d, 2-b, 3-a, 4-c 1-c, 2-a, 3-b, 4-d In designing a computer's cache system, the cache one of the following statements is correct in this cor A smaller block size implies better spatial locality A smaller block size implies a smaller cache tag and hence A smaller block size implies a larger cache tag and hence A smaller block size incurs a lower cache miss penalty An IP router with a Maximum Transmission Unit (M bytes with an IP header of length 20 bytes. The value fragment generated by the router for this packet are MF bit: 0, Datagram Length: 1444; Offset: 370 MF bit: 1, Datagram Length: 1424; Offset: 185 | e lower cache tag overhead lower cache hit time TU) of 1500 bytes has received an IP packet of size 4404 es of the relevant fields in the header of the third IP |
| Alt3 Alt4 72 Alt1 Alt2 Alt3 Alt4 73 Alt1 Alt2 Alt3 | 1-d, 2-b, 3-a, 4-c 1-c, 2-a, 3-b, 4-d In designing a computer's cache system, the cache one of the following statements is correct in this cor A smaller block size implies better spatial locality A smaller block size implies a smaller cache tag and hence A smaller block size implies a larger cache tag and hence A smaller block size incurs a lower cache miss penalty An IP router with a Maximum Transmission Unit (M bytes with an IP header of length 20 bytes. The value fragment generated by the router for this packet are MF bit: 0, Datagram Length: 1444; Offset: 370 MF bit: 1, Datagram Length: 1500; Offset: 370 | e lower cache tag overhead lower cache hit time TU) of 1500 bytes has received an IP packet of size 4404 es of the relevant fields in the header of the third IP |
| Alt3 Alt4 72 Alt1 Alt2 Alt3 Alt4 73 Alt1 Alt2 Alt3 | 1-d, 2-b, 3-a, 4-c 1-c, 2-a, 3-b, 4-d In designing a computer's cache system, the cache one of the following statements is correct in this cor A smaller block size implies better spatial locality A smaller block size implies a smaller cache tag and hence A smaller block size implies a larger cache tag and hence A smaller block size incurs a lower cache miss penalty An IP router with a Maximum Transmission Unit (M bytes with an IP header of length 20 bytes. The value fragment generated by the router for this packet are MF bit: 0, Datagram Length: 1444; Offset: 370 MF bit: 1, Datagram Length: 1424; Offset: 185 | e lower cache tag overhead lower cache hit time TU) of 1500 bytes has received an IP packet of size 4404 es of the relevant fields in the header of the third IP |
| Alt3 Alt4 72 Alt1 Alt2 Alt3 Alt4 73 Alt1 Alt2 Alt3 Alt4 | 1-d, 2-b, 3-a, 4-c 1-c, 2-a, 3-b, 4-d In designing a computer's cache system, the cache one of the following statements is correct in this cor A smaller block size implies better spatial locality A smaller block size implies a smaller cache tag and hence A smaller block size implies a larger cache tag and hence A smaller block size incurs a lower cache miss penalty An IP router with a Maximum Transmission Unit (M bytes with an IP header of length 20 bytes. The value fragment generated by the router for this packet are MF bit: 0, Datagram Length: 1444; Offset: 370 MF bit: 1, Datagram Length: 1500; Offset: 370 | e lower cache tag overhead lower cache hit time TU) of 1500 bytes has received an IP packet of size 4404 es of the relevant fields in the header of the third IP e |
| Alt3 Alt4 72 Alt1 Alt2 Alt3 Alt4 73 Alt1 Alt2 Alt3 Alt4 74 | 1-d, 2-b, 3-a, 4-c 1-c, 2-a, 3-b, 4-d In designing a computer's cache system, the cache one of the following statements is correct in this corner A smaller block size implies better spatial locality A smaller block size implies a smaller cache tag and hence A smaller block size implies a larger cache tag and hence A smaller block size incurs a lower cache miss penalty An IP router with a Maximum Transmission Unit (M bytes with an IP header of length 20 bytes. The value fragment generated by the router for this packet are MF bit: 0, Datagram Length: 1444; Offset: 370 MF bit: 1, Datagram Length: 1424; Offset: 370 MF bit: 0, Datagram Length: 1500; Offset: 370 MF bit: 0, Datagram Length: 1424; Offset: 2960 | e lower cache tag overhead lower cache hit time TU) of 1500 bytes has received an IP packet of size 4404 es of the relevant fields in the header of the third IP e |
| Alt3 Alt4 72 Alt1 Alt2 Alt3 Alt4 73 Alt1 Alt2 Alt3 Alt4 74 Alt1 | 1-d, 2-b, 3-a, 4-c 1-c, 2-a, 3-b, 4-d In designing a computer's cache system, the cache one of the following statements is correct in this cor A smaller block size implies better spatial locality A smaller block size implies a smaller cache tag and hence A smaller block size implies a larger cache tag and hence A smaller block size incurs a lower cache miss penalty An IP router with a Maximum Transmission Unit (M bytes with an IP header of length 20 bytes. The value fragment generated by the router for this packet are MF bit: 0, Datagram Length: 1444; Offset: 370 MF bit: 1, Datagram Length: 1500; Offset: 370 MF bit: 0, Datagram Length: 1424; Offset: 2960 Which one of the following protocols is NOT used to | e lower cache tag overhead lower cache hit time TU) of 1500 bytes has received an IP packet of size 4404 es of the relevant fields in the header of the third IP e |

75 The minimum number of JK flip-flops required to construct a synchronous counter with the count sequence (0,0,1,1,2,2,3,3,0,0,...) is

Alt4 RARP

| Alt1 | 2 |
|------|--|
| Alt2 | |
| Alt3 | |
| Alt3 | |
| AIL4 | 32 |
| 76 | Using Demorgan's theorem we can convert any AND-OR structure into |
| Alt1 | NAND-NAND |
| Alt2 | OR-NAND |
| Alt3 | NAND –NOR |
| | NOR-NAND |
| | |
| 77 | Which group of instructions does not affect the flags? |
| Alt1 | Arithmetic operations |
| Alt2 | Logic operations |
| Alt3 | Data transfer operations |
| | Branch operations |
| | |
| 78 | Consider a hash table with 100 slots. Collisions are resolved using chaining. Assuming simple uniform hashing, |
| | what is the probability that the first 3 slots are unfilled after the first 3 insertions? |
| | |
| Alt1 | $(97 \times 97 \times 97)/1003$ |
| Alt2 | $(99 \times 98 \times 97)/1003$ |
| Alt3 | $(97 \times 96 \times 95)/1003$ |
| Alt4 | (97 × 96 × 95)/(3! × 1003) |
| | |
| 79 | The transport layer protocols used for real time multimedia, file transfer, DNS and email, respectively are |
| Alt1 | TCP, UDP, UDP and TCP |
| Alt2 | UDP, TCP, TCP and UDP |
| Alt3 | UDP, TCP, UDP and TCP |
| Alt4 | TCP, UDP, TCP and UDP |
| | |
| 80 | A computer uses 46-bit virtual address, 32-bit physical address, and a three-level paged page table organizatio |
| | The page table base register stores the base address of the first-level table (T1), which occupies exactly one |
| | page. Each entry of T1 stores the base address of a page of the second-level table (T2). Each entry of T2 stores |
| | the base address of a page of the third-level table (T3). Each entry of T3 stores a page table entry (PTE). The PT |
| | is 32 bits in size. The processor used in the computer has a 1 MB 16-way set associative virtually indexed |
| | physically tagged cache. The cache block size is 64 bytes |
| | |
| | What is the size of a page in KB in this computer? |
| Alt1 | 2 |
| Alt2 | 4 |
| Alt3 | 8 |
| | 16 |

A computer uses 46-bit virtual address, 32-bit physical address, and a three-level paged page table organization. The page table base register stores the base address of the first-level table (T1), which occupies exactly one page. Each entry of T1 stores the base address of a page of the second-level table (T2). Each entry of T2 stores the base address of a page of the third-level table (T3). Each entry of T3 stores a page table entry (PTE). The PTE is 32 bits in size. The processor used in the computer has a 1 MB 16-way set associative virtually indexed physically tagged cache. The cache block size is 64 bytes

What is the minimum number of page colours needed to guarantee that no two synonyms map to different sets in the processor cache of this computer?

Alt1 2

Alt2 4

Alt3 8

Alt4 16

| 82 | A bit-stuffing based framing protocol uses an 8-bit delimiter pattern of 01111110. If the output bit-string after |
|------|---|
| | stuffing is 01111100101, then the input bit-string is |
| Alt1 | 111110100 |

7111110100

Alt2 111110101

Alt3 111111101

Alt4 111111111

83 What is the output of the following C code

```
Assume that the address of x is 2000(in decimal) and an integer requires 4 bytes of memory int main() {
    unsigned int x[4][3]= { {1,2,3}, {4,5,6}, {7,8,9}, {10,11,12} };
    printf(" %u %u %u", x+3, *(x+3), *(x+2)+3);
    }
```

What is the output of the following C code

Assume that the address of x is 2000(in decimal) and an integer requires 4 bytes of memory

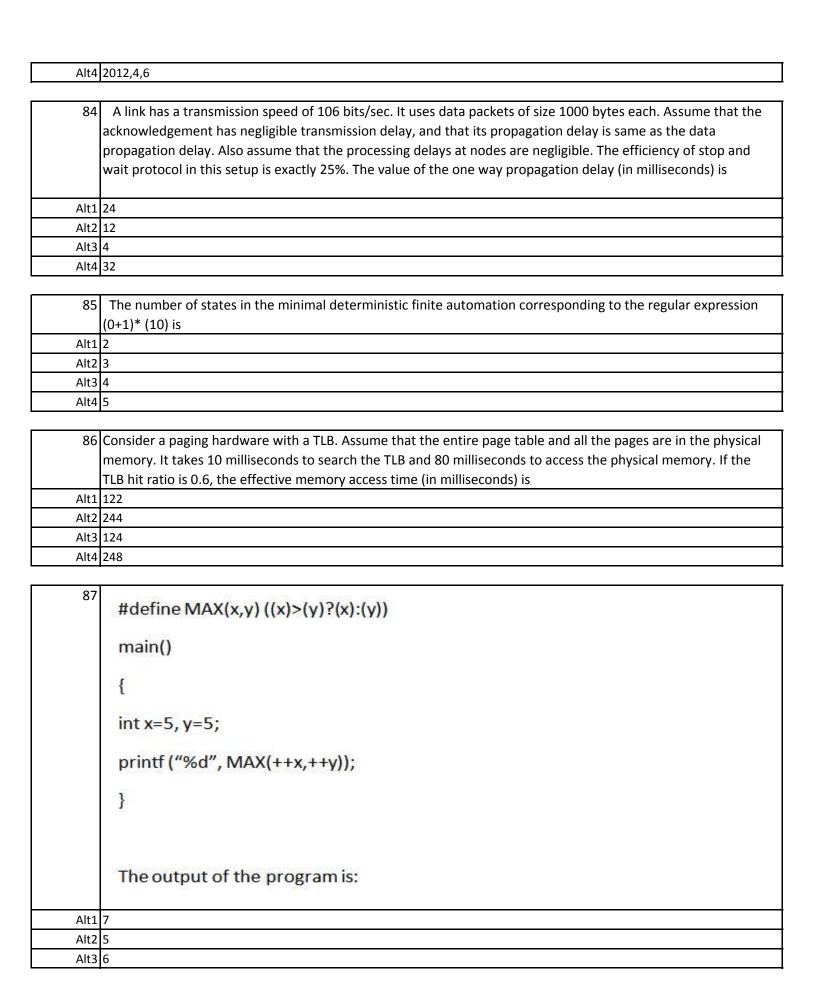
```
int main() {
```

```
unsigned int x[4][3]= { {1,2,3}, {4,5,6}, {7,8,9}, {10,11,12} };
printf("%u%u%u", x+3, *(x+3), *(x+2)+3);
}
```

| Alt1 | 2.0362E+11 |
|------|------------|
|------|------------|

Alt2 2012,4,2204

Alt3 2036, 10,10



Alt4 99

```
Given the following definitions, what will be the value of r?
int *p, *q, r;
int values[30];
p=&values[0];
q=values+29;
r=++q-p;

Alt1 address of q minus p
Alt2 number of elements in the array
Alt3 (value pointed by q)+1-(value pointed by p)
Alt4 qp
```

```
What will be the output of the program? #include <stdio.h>

static int =5;

main()

{

int sum=0;

do

{

sum+=(1/i);

}while(0<i--);

printf ("%d", sum);

}

Alt1 sum of the series is printed

Alt2 compilation error

Alt3 runtime error
```

Alt4 typo error

```
#include <stdio.h>
enum mode={green, red, orange, blue, white};
main()
{
green = green+1;
printf ("%d"%d",green,red);
}
The output of the program will be:

Alt1 1,1
Alt2 0,1
Alt3 no output, error in compilation
Alt4 1,2
```

```
What is the size of ptr1 and ptr2?

Int j;

Char k[100];

Unsigned I;

j;

int *ptr1;

struct x * ptr2;

Alt1 same

Alt2 2, 104

Alt3 2, undefined for memory is not allowed

Alt4 2, 4
```

```
92
       What is the output of the following program?#include <stdio.h>
       main(0
      {
       int i=0;
      switch(i)
      {
       case 0: i++;
      case 1: i++2;
      case 2: ++i;
      }
       printf ("%d", i++);
      The output of the program is:
Alt1 1
Alt2 3
Alt3 4
Alt4 5
```

```
93 If i=5, what is the output for printf ("%d%d%d", ++i,i,i++)?

Alt1 5,6,7

Alt2 6,6,7

Alt3 7,6,5

Alt4 6,5,6
```

```
For the following code, how many times is the printf function executed?

int i,j;

for (i=0;i<=10;i++);

for (j=0;j<=10;j++);

printf("i=%d,j=%d\n",i,j);
```

| Alt2 | 11 |
|------|-----|
| Alt3 | 10 |
| Alt4 | 129 |

| | What is the output generated for the following code? #define square (a) (a*a) printf("%d",square(4+5)); |
|------|---|
| Alt1 | 81 |
| Alt2 | 4 |
| Alt3 | 29 |
| Alt4 | 18 |

```
For the following statement, find the values generated for p and q.
int p=0, q=1;
p=q++;
p=++q;
p=-q;
p=-q;
Alt1 1,1
Alt2 0,0
Alt3 3,2
Alt4 1,2
```

```
What is the output generated by the following program? #include <stdio.h>
      main()
      int a, count;
     int func(int);
     for(count=1;count<=5;++count)
     {
      a=func(count);
      printf("%d",a);
     }}
      int func(int x)
     {
      int y;
      y=x*x;
      return (y);
     }
Alt1 1234567
Alt2 2516941
Alt3 9162514
Alt4 1491625
```

```
98 How many X's are printed? for (i=0;j=10;i<j;i++,j--)
printf("X");

Alt1 10
Alt2 5
Alt3 4
Alt4 45
```

| 99 | 99 In a signed magnitude notation, what is the minimum value that can be represented with 8 bits? | | | | | |
|------|---|--|--|--|--|--|
| Alt1 | -128 | | | | | |
| Alt2 | -255 | | | | | |
| Alt3 | -127 | | | | | |
| Alt4 | 0 | | | | | |

```
Write one statement equivalent to the following two statements: x=sqr(a); return(x);

Alt1 return(sqr(a));
```

| <i>A</i> | printf("sqr(a)"); |
|----------|----------------------|
| <i>A</i> | return(a*a*a); |
| - | printf("%d",sqr(a)); |